Design of Interdigitated Capacitors and Their Application to Gallium Arsenide Monolithic Filters

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Abstract—**Theoretical expressions for the interelectrode capacitance and conductor losses for an array of microstrip transmission lines are presented. The effect of finite conductor thickness is included in the analysis by introducing equations for the effective width of the transmission lines. Good agreement between theory and experiment is observed up to 18 GHz. Experimental results obtained from a lumped-element GaAs monolithic bandpass filter are in excellent agreement with theory. The filter has 1.5-dB insertion loss at 11.95 GHz and greater than 22-dB loss in the stopband. The filter measures $0.58 \times 1.3 \times 0.203$ mm.**

I. INTRODUCTION

A MAJOR TASK in the development of gallium arsenide (GaAs) monolithic circuits is the careful analysis and design of lumped-element microwave components. This paper presents design considerations and experimental results for lumped-element interdigital capacitors fabricated on GaAs semi-insulating substrates. The lumped capacitor is formed by the fringing field of an interdigital gap between fingers. Because of size limitations, the capacitance values obtained are typically less than 1 pF.

Interdigital capacitors have proven to be useful components in GaAs monolithic integrated circuits due to their simplicity of construction, relatively high Q, and repeatability. Their use affords a considerable size reduction when compared with equivalent distributed matching structures and they are higher yield, lower loss, and more repeatable than overlay capacitors.

In Section II, an analysis of interdigital capacitors is presented. In previous works [1], [2], the authors have used single-strip microstrip losses in their analysis. This approach significantly underestimates the losses of the odd-mode component. In the present technique, the loss components α_e and α_o are calculated for an array of microstrip lines by applying the incremental inductance rule [3]. The effect of finite strip thickness is also considered in the analysis which gives results that agree well with experiment. In Section III, a derivation of loss factors is presented. From these formulas the loss of a microstrip line in an array of lines is obtained for a given conductor thickness. The conductor loss equations are presented in terms of the fringing and parallel-plate capacitance of the microstrip lines, which make it very convenient for use in a computer-aided design approach. To support the theoretical analysis, several interdigital capacitors have been designed and fabricated on GaAs semi-insulating substrates. The fabricated devices have been tested on a semi-automatic network analyzer over the 2- to 18-GHz frequency range. In Section IV, the experimental results are presented and compared to the theory. A monolithic two-pole bandpass filter is presented in Section V. Finally, Section VI summarizes the results.

Manuscript received April 29, 1982; revised August 2, 1982.

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II. THEORETICAL ANALYSIS

Consider the interdigital capacitor depicted in Fig. 1. For the purpose of analysis, let us disregard the fingers and consider their effects later in the calculation. The two terminal strips can be regarded as a pair of coupled microstrip transmission lines and a four-port admittance matrix may be calculated using the theory of coupled transmission lines in an inhomogeneous media [4]. In the case of a center-tapped capacitor, where neither end of the terminal strips is grounded, if one assumes ports 1, 2, 3, and 4 are open circuited, then the impedance matrix for each half section is given by

$$Z''_{11} = Z''_{22} = \frac{1}{2}\left[Z_{Te}\coth(\gamma_{Te}l_T/2) + Z_{To}\coth(\gamma_{To}l_T/2)\right] \tag{1}$$

$$Z''_{21} = Z''_{12} = \frac{1}{2}\left[Z_{Te}\coth(\gamma_{Te}l_T/2) - Z_{To}\coth(\gamma_{To}l_T/2)\right] \tag{2}$$

$$y'_{T11} = 2y''_{11} \tag{3a}$$

$$y'_{T12} = 2y''_{12}. \tag{3b}$$

y_{T11}, y_{T12} are the elements of the matrix where $[Y_T] = [Z_T]^{-1}$ and l_T is the length of the terminal strip. For the end-tapped configuration where ports 2 and 4 are open circuited, the impedance matrix is

$$Z_{T11} = Z_{T23} = \frac{1}{2}\left[Z_{Te}\coth(\gamma_{Te}l_T) + Z_{To}\coth(\gamma_{To}l_T)\right] \tag{3}$$

$$Z_{T31} = Z_{T13} = \frac{1}{2}\left[Z_{Te}\operatorname{csch}(\gamma_{Te}l_T) - Z_{To}\operatorname{csch}(\gamma_{To}l_T)\right]. \tag{4}$$

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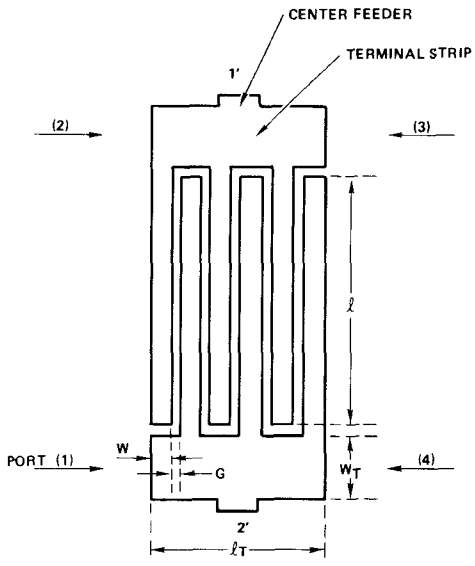


Fig. 1. Top view of an interdigital capacitor.

Now the task is to calculate the characteristic impedances Z_{Te}, Z_{To} and propagation constants γ_{Te}, γ_{To} for the terminal strip taking the effects of the fingers into consideration. We assume that the capacitor dimensions are much less than a quarter of a wavelength, and the fingers can be represented by an effective distributed shunt admittance across the terminal strip. Therefore, at a specified angular frequency ω, the characteristic admittance and propagation constant for the terminal strip are given by

$$Z_{Te} = \sqrt{\frac{R_T + j\omega L_{Te}}{j\omega C_{Te} + N_F(y_{11} + y_{21})/2l_T}} \tag{4}$$

$$Z_{To} = \sqrt{\frac{R_T + j\omega L_{To}}{j\omega C_{Te} + N_F(y_{11} - y_{21})/2l_T}} \tag{5}$$

$$\gamma_{Te} = \sqrt{(R_T + j\omega L_{Te})[j\omega C_{Te} + N_F(y_{11} + y_{21})/2l_T]} \tag{6}$$

$$\gamma_{To} = \sqrt{(R_T + j\omega L_{To})[j\omega C_{To} + N_F(y_{11} - y_{21})/2l_T]} \tag{7}$$

where C_{Te}, C_{To}, L_{Te}, and L_{To} represent the even- and odd-mode capacitances and inductances for the terminal strip, R_T is the resistance of the conductors, and N_F is the number of fingers. y_{11} and y_{21} are the elements of the admittance matrix for $N_F/2$ interdigital sections in parallel. These admittances are averaged over the terminal strip length in the above formulas. The values of y_{11} and y_{21} can be calculated as follows: Assuming each two-finger pair forms a system of coupled transmission lines, open circuited at opposite ends, one can deduce the matrix y from the theory of coupled transmission lines in an inhomogeneous media [4]. Therefore

$$Z_{11} = Z_{22} = \frac{1}{2}[Z_{oe}\coth\gamma_e l + Z_{oo}\coth\gamma_o l] \tag{8}$$

$$Z_{21} = Z_{12} = \frac{1}{2}[Z_{oe}\operatorname{csc}\gamma_e l - Z_{oo}\operatorname{csc}\gamma_0 l] \tag{9}$$

$$[Y] = [Z]^{-1} \tag{10}$$

where Z_{oo}, Z_{oe}, γ_o, and γ_e are the odd- and even-mode impedances and propagation constants of the fingers, and l is the length of overlap of the fingers. The impedances Z_{oo}, Z_{oe} are calculated by obtaining the total capacitance of finger. The total capacitance is the summation of parallel-plate and fringing capacitances. The fringing capacitance is computed by applying a theoretical technique given by Smith [5]. The fringing capacitance for each finger is calculated by considering the effect of the immediately adjacent fingers. The loss factors α_o and α_e for the propagation constant γ_o, γ_e are calculated in the following section.

III. Conductor Losses

The even- and odd-mode attenuation constant due to ohmic losses for coupled microstrip lines can be determined using the incremental inductance rule of Wheeler [3]. Hence

$$\alpha = \frac{R_s}{2Z_0\mu_0}\frac{\delta L}{\delta n} \tag{10}$$

where R_s is the surface resistivity, δL is the change in the inductance that occurs when all cross-sectional conductors are perturbed by a distance δn inward, normal to the conductor surface (Fig. 2). In this case, it is more convenient to write (10) in terms of capacitance

$$\alpha = \frac{R_s}{2Z_0\eta c C^{a^2}}\frac{\delta C^a}{\delta n} \tag{11}$$

where η is the free-space impedance, c is the velocity of light, and C^a is the total capacitance of microstrip with air as dielectric. C^a is a function of h, the distance between conductors and ground plane, G the gap spacing between the neighboring conductors, and t and w the thickness and width of the conductor, respectively (see Fig. 2). By considering to first order the variation in capacitance that occurs due to an inward normal perturbation δn at each surface, there results

$$\delta h = \delta G = +2\,\delta n$$
$$\delta w = \delta t = -2\,\delta n.$$

The variation in C^a is

$$\delta C^a = \frac{\partial C^a}{\partial h}\delta h + \frac{\partial C^a}{\partial t}\delta t + \frac{\delta C^a}{\partial w}\delta w + \frac{\partial C^a}{\partial G}\delta G \tag{12}$$

and furthermore

$$C^a = C_p^a + C_f^a$$

where $C_p^a = \epsilon_0 w/h$ is the total parallel-plate capacitance in picofarads per centimeter and C_f is the fringing capacitance. Then α_o for the odd mode can be written as

$$\alpha_o = \frac{R_s}{Z_{00}\eta c C^{a^2}}\left[\frac{\epsilon_0 w}{h^2} + \frac{\epsilon_0}{h}\left(1 + \frac{\partial w}{\partial t}\right) - \frac{\partial C_{f0}^a}{\partial h} - \frac{\partial C_{f0}^a}{\partial G} + \frac{\partial C_{f0}^a}{\partial w}\left(1 + \frac{\partial w}{\partial t}\right)\right]. \tag{13}$$

A similar expression holds for the even-mode attenuation constant.

When the microstrip conductor is of finite thickness t, the impedance can be evaluated by using the concept of

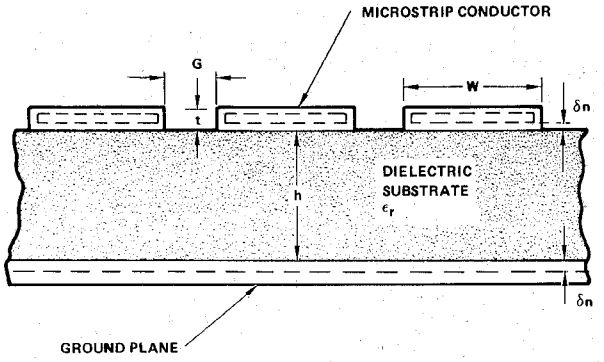


Fig. 2. An array of coupled microstrip line cross section showing an inward perturbation of an all metal surface.

effective width to obtain $\partial w/\partial t$. An expression for effective width W^t has been obtained by Jansen [6] for coupled microstrip lines. Similar expressions have been found to work well for an array of microstrip lines

$$W_e^t = W + \Delta W\left[1 - \exp(-A)\right] \tag{14}$$

$$W_o^t = W_e^t + \Delta t \tag{15}$$

where

$$\Delta t = \frac{2h}{\epsilon_r}\frac{t}{G} \tag{16}$$

$$A = 0.35\frac{\Delta w}{\Delta t} \tag{17}$$

and Δt is the increase in effective width for the odd mode when compared with the even mode. This increase Δt has been approximated by modeling the excess capacitance, over the $t = 0$ case, by parallel-plate capacitance. The constants have been determined by a fit to the measured results. The error in the above approximations increases for $G > t$.

An expression for Δw the effective increase in microstrip width of single microstrip transmission line due to strip thickness is given approximately by Wheeler and Hughes *et al.*, [3], [7], [8], and is repeated below

$$\Delta w = \frac{t}{\pi}\left(1 + \ln\frac{4\pi w}{t}\right), \qquad \frac{w}{h} \leqslant \frac{1}{2\pi}$$

$$\Delta w = \frac{t}{\pi}\left(1 + \ln\frac{2h}{t}\right), \qquad \frac{w}{h} \geqslant \frac{1}{2\pi}. \tag{18}$$

The partial derivative $\partial w/\partial t$ is obtained by computing $\partial w^t/\partial t$ from (14) and (15). The result for the even mode is

$$\frac{\partial w^e}{\partial t} = \frac{\partial \Delta w}{\partial t}\left[1 - (1 + A)\exp(-A)\right] + \frac{2A^2 h}{\epsilon_r G}\exp(-A) \tag{19}$$

and for the odd mode is

$$\frac{\partial w^o}{\partial t} = \frac{\partial w^e}{\partial t} + \frac{2h}{\epsilon_r G} \tag{20}$$

where

$$\frac{\partial \Delta w}{\partial t} = \frac{1}{\pi}\ln\left(\frac{4\pi w}{t}\right), \qquad \frac{w}{h} \leqslant \frac{1}{2\pi}$$

$$= \frac{1}{\pi}\ln\left(\frac{2h}{t}\right), \qquad \frac{w}{h} \geqslant \frac{1}{2\pi}. \tag{21}$$

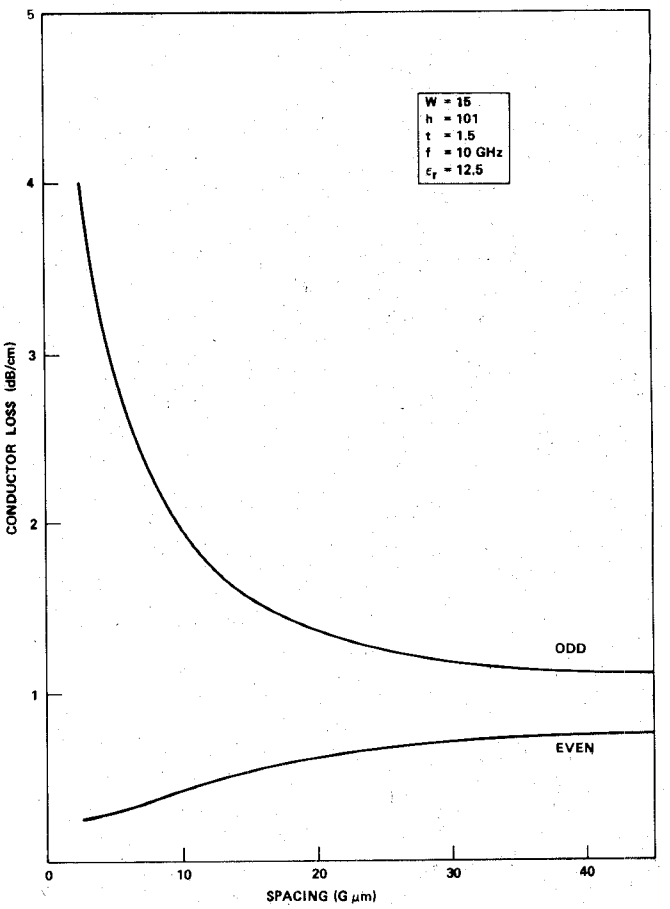


Fig. 3. Even- and odd-mode conductor losses in a microstrip array as a function of finger gap spacing.

Utilizing (19) and (20), the values of α_o and α_e are calculated from (13).

The derivatives in (13) were evaluated by applying a finite-difference approximation with the grid dimension taken to be several skin depths. In all of the following calculations, the resistivity of the conductor is assumed to be 3×10^{-6} Ω·cm and all dimensions are in micrometers. Results for a microstrip line in an array of microstrip lines are calculated by considering the effect of closest neighboring strip lines. Fig. 3 shows a plot of α_o and α_e as a function of conductor spacing for a microstrip in an array of microstrip lines. The conducting material is Cr–Au on a 0.1-mm-thick GaAs substrate. The even-mode attenuation constant is always less than the odd-mode value. The even-mode losses approach those of an infinite conducting sheet above a ground plane as the gap spacing approaches zero. Both even- and odd-mode losses approach those of a single isolated microstrip line for large spacing. Dielectric losses are neglected in these calculations since the loss tangent of semi-insulating GaAs is $2\text{–}3 \times 10^{-4}$ in the 2–12-GHz frequency range, which gives a dielectric loss of less than 0.015 dB/in. The variation of conductor attenuation for an array of lines as a function of finger width is shown in Fig. 4. Note that for finger width less than 10 μm, the odd-mode conductor losses increase sharply. The even-mode losses stay approximately constant for finger widths above 15 μm. This value is approximately equal to the loss of an infinite conducting sheet above a ground plane. For

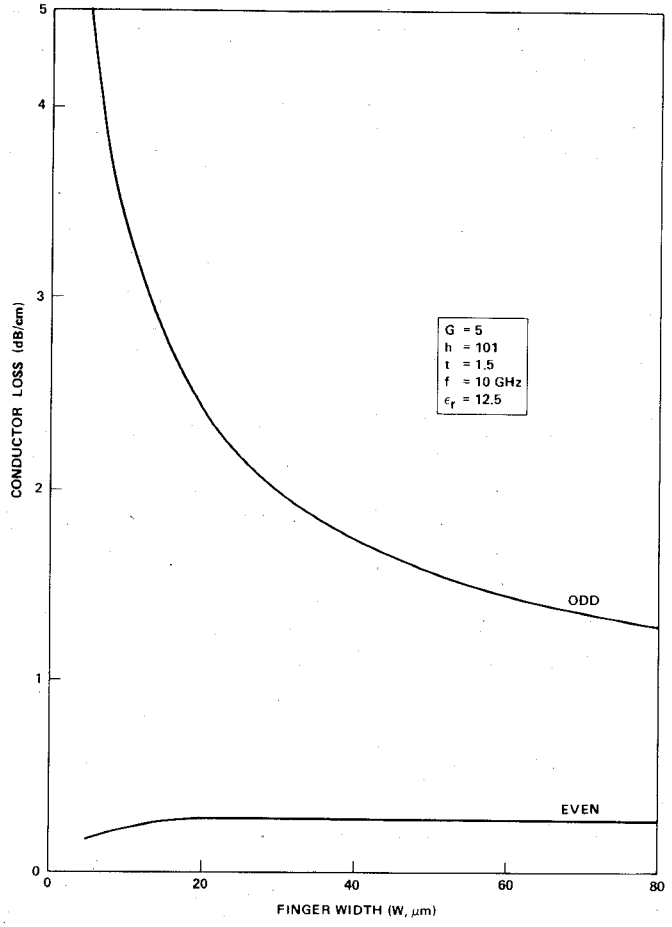


Fig. 4. Even- and odd-mode conductor losses in a microstrip array as a function of strip width.

small finger width ($w < 10$ μm) even-mode losses decrease due to a decrease in even-mode capacitance. Also Fig. 3 indicates that conductor spacings of less than 5 μm have a substantial effect on odd-mode losses. Although larger finger width and wider spacing reduce the overall conductor losses, it increases the parasitic capacitance and increases the physical size of the device.

IV. Theoretical and Experimental Results

Several interdigital capacitors of different values were designed and processed on semi-insulating GaAs substrates using high-resolution photolithographic techniques. Several of these capacitors were resonated with a high-impedance microstrip line to facilitate high-frequency Q measurement. The S-parameters of the devices were measured using an HP 8409A semiautomatic network analyzer over the 2–18-GHz frequency range. Fig. 5 shows a picture of one of the devices assembled on a test fixture. Equations (1)–(10) with the aid of (13) were used to calculate the Y-parameters for a number of interdigital capacitors. The Y-parameters were then converted to S-parameters for comparison with experimental results. Fig. 6(a) and (b) shows the calculated and measured S-parameters for two interdigital capacitors which will be designated by CAP 1 and CAP 2, respectively. The dimensions are given on the figure. The parasitic inductances which are associated with the bond-

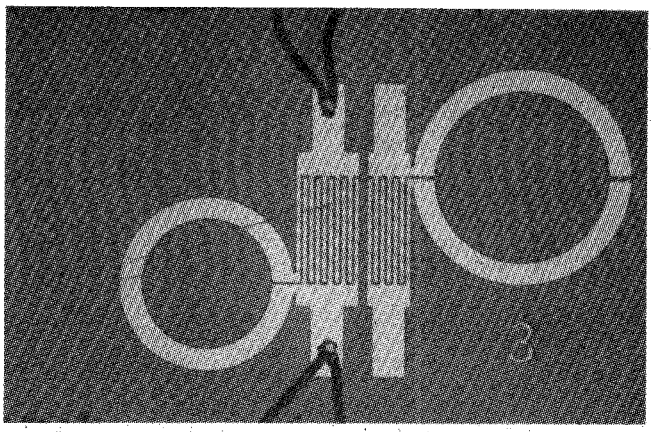
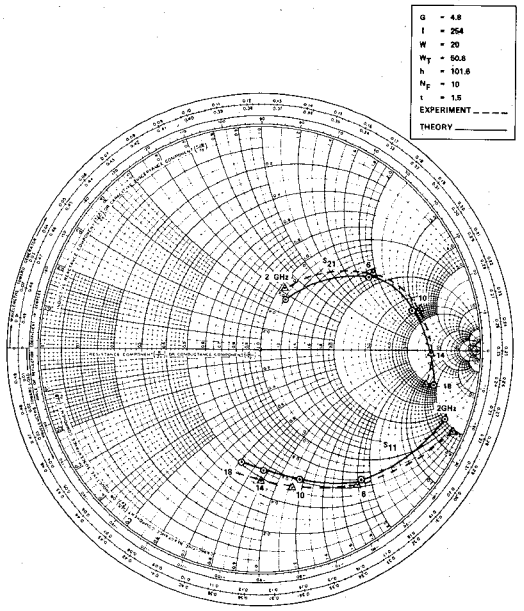
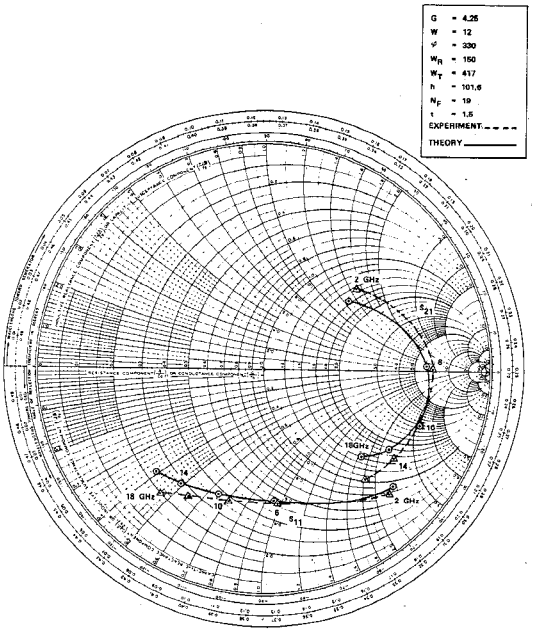


Fig. 5. A resonance test structure for interdigital capacitor testing.



(a)



(b)

Fig. 6. Measured and theoretical S-parameters for two samples of interdigital capacitors. (a) CAP 1 and (b) CAP 2.

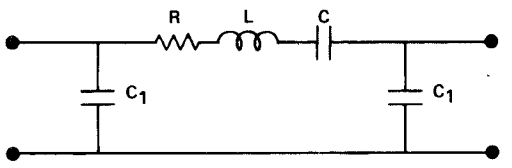


Fig. 7. Equivalent circuit model for interdigital capacitors.

TABLE I
EXPERIMENTAL AND THEORETICAL ELEMENTS VALUES FOR THE CIRCUIT MODEL OF FIG. 7 FOR TWO SAMPLES OF INTERDIGITAL CAPACITOR

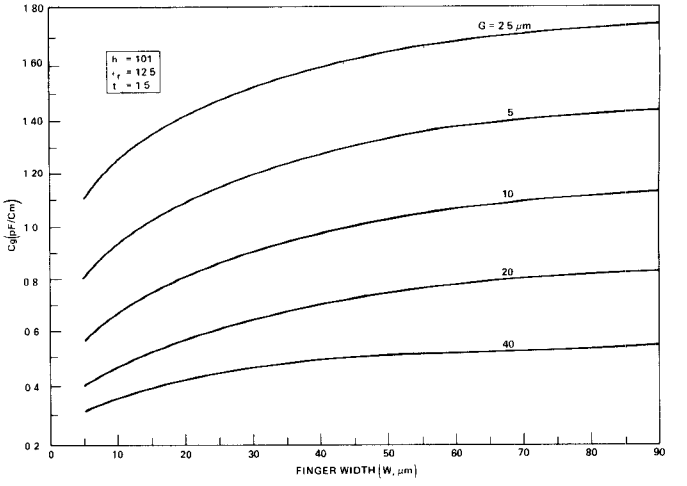
CAP 1	R (Ω)	L (nH)	C (pF)	C_1 (pF)
1*			0.248	0.092
2	1	0.065	0.247	0.075
3	1.122	0.167	0.242	0.073
CAP 2				
1			0.609	0.100
2	1.019	0.076	0.607	0.149
3	1.062	0.173	0.590	0.177

*1—Calculated static capacitance. 2—From measured *S*-parameters. 3—From coupled line theory.

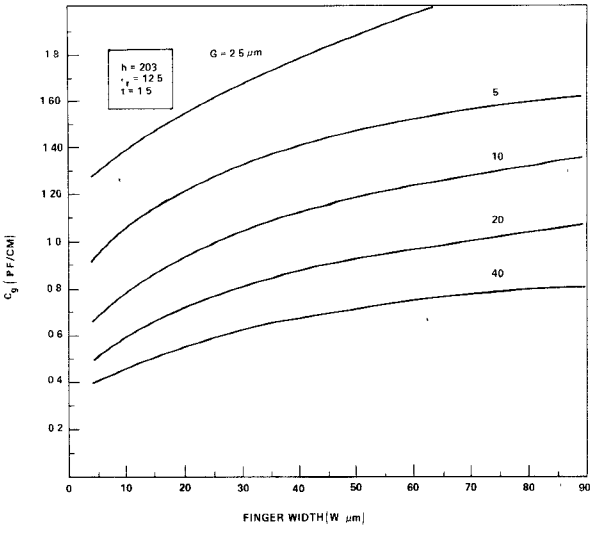
ing wires are extracted from the measured *S*-parameters data presented in Fig. 6(a) and (b). The measured *S*-parameters were fitted using a least squares error technique to the circuit model presented in Fig. 7. Fig. 6(a) and (b) indicates good correlation between experiment and theory. Table I presents the element values of the device equivalent circuit (Fig. 7) obtained by data-fitting techniques from the measured and calculated *S*-parameters over the frequency range of 2–18 GHz. These data are presented for the capacitors CAP 1 and CAP 2 for which the *S*-parameters are given in Fig. 6(a) and (b). The static capacitance is also presented. The values of static gap capacitance for both a 4- and an 8-mil-thick substrates with various line separation and finger widths are plotted in Fig. 8(a) and (b). These curves are obtained from coupled line theory (5) where calculation of even- and odd-mode fringing capacitances for coupled lines is made for finite line widths assuming a periodic array of lines. The effect of thickness is also considered in Fig. 8. The thickness effect makes a substantial difference for small finger spacing. From Fig. 8, the capacitance C can simply be calculated by

$$C = (N_F - 1)Cg \cdot l.$$

These plots are helpful for designing interdigital capacitors with optimum aspect ratios which will be discussed in the next section. The value of capacitance C_1 in Fig. 7 is the summation of parallel-plate capacitance and the even-mode fringing capacitance to ground. The Q of the interdigital capacitors was measured for several devices. The unloaded Q obtained by a resonance technique is between 35 and 45 for the combined *LC* microstrip circuit at 12–14 GHz. One can extract the measured Qc for the interdigital capacitor if an *RLC* circuit model is assumed for the combined resonance circuit shown in Fig. 5. By use



(a)



(b)

Fig. 8. Static gap capacitance values for different finger widths and gaps on GaAs semi-insulating substrates. (a) $h = 101$ μm and (b) $h = 203$ μm.

of this technique, Qc's in excess of 60 at 8 GHz were obtained for some of the devices which were tested.

Another technique for obtaining Q is from the circuit model of Fig. 7. This can be done after the measured and calculated *S*-parameters are fitted to the circuit model of Fig. 7. Fig. 9 presents the Q-values verses of frequency for an interdigital capacitor (CAP 2) obtained using such a technique. This method gives a better agreement with the theory which is also plotted in Fig. 9. Fig. 10 shows the effect of conductor thickness on capacitance values. For this particular example there is about an 11-percent difference between the capacitance at zero thickness and for a 2-μm-thick conductor. A design knowledge of the minimum acceptable thickness of strip would be an advantage in the fabrication of microstrip circuits, in that, the thinner the strip used, the less undercutting of line would be experienced during etching. Also, it would be easier to maintain the integrity of device dimensions and less costly. Horton *et al.* [9] and later Rizzoli [10] have shown theoreti-

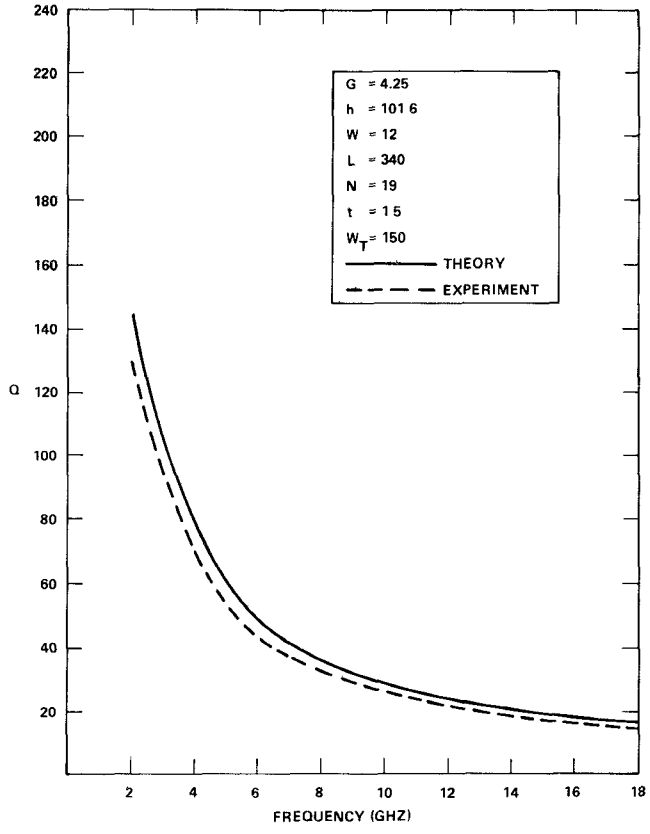


Fig. 9. Variation of Q as function of frequency for a 0.602-pF capacitance.

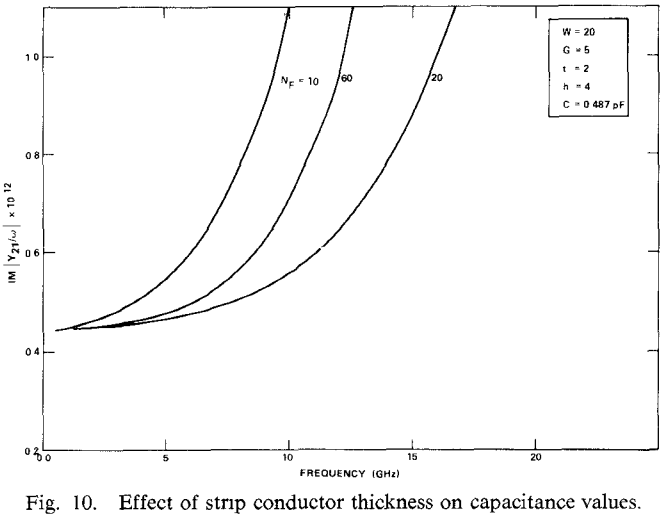


Fig. 10. Effect of strip conductor thickness on capacitance values.

cally that losses increase as $t \to 0$ for single microstrip lines and an absolute minimum exists for $t = \delta$, where δ is the skin depth. They argue that there exists an optimum strip thickness of approximately three times the skin depth for lowest loss. For a gold conductor this thickness is about 2.4 μm at 10 GHz. Equations (13)–(21) show a sharp increase for both even- and odd-mode losses for conductor thicknesses below 2 μm. An extensive experimental study on optimum conductor thickness has not been done but Q-measurements for two different metallization thicknesses

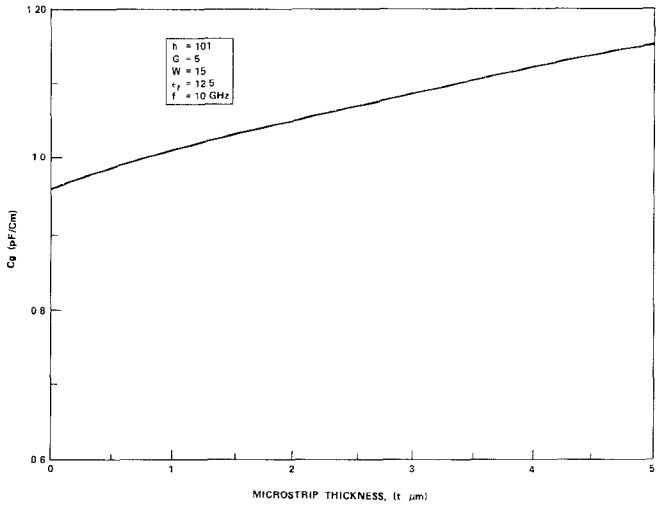


Fig. 11. Variation of the imaginary part of Y_{21} as a function of frequency for a 0.487-pF capacitor for various number of fingers.

were performed. A reduction in Q_u of more than 50 percent was measured when metallization thickness was reduced from 1.5 to 0.7 μm. The effect of the metal thickness on losses was also observed on the insertion-loss measurement done on the bandpass filter which will be discussed in the next section. Another important consideration is the dependence of capacitance values on frequency. The theoretical calculation indicates that the value of capacitance varies with frequency due to the change in finger length l and terminal strip length w_T. The optimum ratio of w_T/l for a specific capacitance corresponds to a minimum in $\partial C/\partial f$, where f is frequency. For series-connected interdigital capacitors, the capacitance slope is proportional to the slope of the imaginary part of y_{21}/ω. Fig. 11 is a plot of IM (y_{21}/ω) versus frequency for a 0.487-pF capacitance for different w_T/l ratios. It is apparent that a minimum slope exists for various aspect ratios. The search for minimum slope can be done efficiently with a computer-assisted design procedure.

V. Circuit Application

From the above analysis, the following design criteria for interdigitated capacitors on 0.202-mm GaAs substrates have been formulated. For minimal area, select capacitance values of less than 1.0 pF. To reduce losses, choose finger widths larger than or equal to 10 μm and gaps not less than 5 μm. Finally, for minimum dependence of capacitance value on frequency, choose the optimum aspect ratio w_T/l. Based on these criteria, a two-pole 0.5-dB ripple Chebyschev bandpass filter with a 5-percent bandwidth centered at 11.95 GHz was designed and fabricated on a semi-insulating GaAs substrate. Fig. 12(a) and (b) shows the initial circuit and the circuit model used for optimizing the final device layout. Fig. 12(b) shows the initial circuit plus all the parasitics from the lumped-element interdigitated capacitor, physical layout, and connections of each component. The capacitance values were kept to less than 1

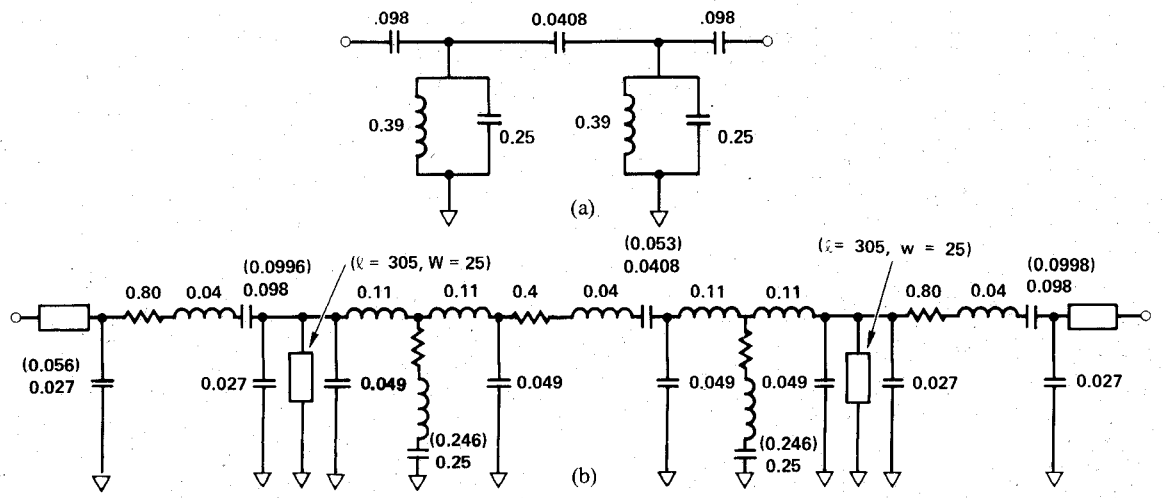


Fig. 12. (a) Equivalent circuit of an *X*-band two-pole bandpass filter. (b) Equivalent circuit with parasitics. Values in parentheses are from measured *S*-parameters. Capacitance and inductance are in picofarads and microhenrys, the dimensions are in micrometers.

pF by applying standard filter design procedures [11]. Before fabricating the final filter, three steps in optimizing the circuit were performed. Since no circuit tuning or tweaking is practical in GaAs monolithic integrated circuits, it is necessary to perform most of the circuit tuning by computer-aided analysis and optimization. The following optimization procedure proved to be effective for the present filter. First, the initial circuit (Fig. 12(a)) was optimized over the frequency band of interest. Next, we included all the parasitics due to interdigital capacitors which could be approximated by the above theory. After inclusion of all of these parasitics the circuit was optimized again. This procedure will adjust the most sensitive parameters to compensate for the effect of the parasitics. The third and final optimization or parameter adjustment comes after the physical layout of the device. Layout parasitics arise, for example, due to extension of sections of microstrip lines for the purpose of physically connecting components. The filter was fabricated using direct-write electron-beam lithography. The capacitors use 15-μm fingers and 5-μm gaps and are formed in 1.5-μm-thick gold on a 0.202-mm semi-insulating GaAs substrate. The filter size is 0.58×1.32 mm. This is an order of magnitude smaller in area than a distributed version of the same filter which was also fabricated. Fig. 13 shows an enlarged picture of the fabricated monolithic filter on GaAs semi-insulating substrate. Fig. 14 shows the response of this filter plotted directly from the output of a semiautomatic network analyzer. The in-band insertion loss is 1.5 dB and the image rejection at 9.5 GHz is greater than 22 dB. The losses were reduced about 0.5 dB by chemically polishing the back of the substrate using a sodium hypochlorite solution before depositing the back metallization. Also we have achieved about 0.5-dB reduction in losses by using thicker plated metallization (about 2.5 μm) over the microstrip portion of the filter. The filter response in Fig. 14 is achieved after polishing and plating thicker gold.

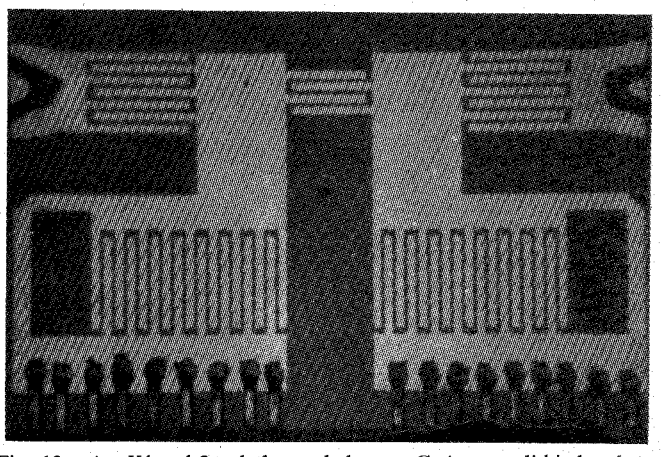


Fig. 13. An *X*-band 2-pole lumped-element GaAs monolithic bandpass filter.

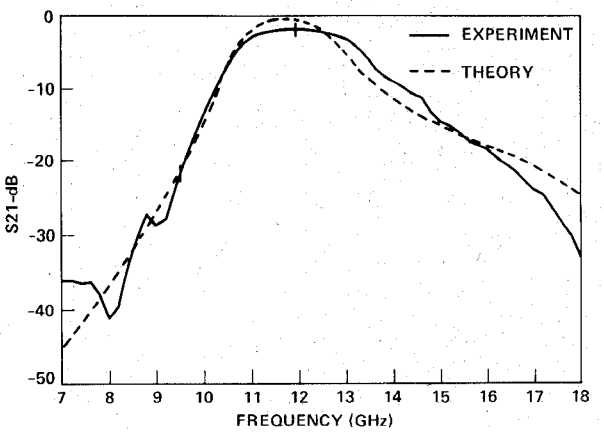


Fig. 14. Measured and theoretical insertion loss of the filter from 2–18 GHz.

VI. Conclusion and Summary

Theoretical expressions for the capacitance and conductor loss for an array of microstrip lines have been presented in a form suitable for interactive computer-aided

design. Conductor losses have been calculated for an array of microstrip transmission lines using the incremental inductance rule. By including the conductor thickness in the analysis, a better correlation between theory and experiment can be achieved. To design an optimum interdigitated capacitor one should first select W and G for maximum Q-values and minimum parasitics. This selection can be aided with curves similar to Figs. 3, 4, and 8. If a minimum dependence of capacitance on frequency is important for an application, a search for minimum variation in capacitance slope may be easily performed. From these analyses, an iterated procedure for designing a monolithic filter on GaAs has been presented. Good correlation between theory and experiment suggests that the interdigital capacitors remain essentially lumped up to 18 GHz. The losses are highly dependent on gap width, finger width, and metallization thickness. Q-values are higher than those of MOM capacitors, however, not as high as reported in an earlier work [1]. Nevertheless, with careful design, reasonable Q's can be achieved for application in monolithic GaAs integrated circuits.

Acknowledgment

The authors wish to acknowledge the support of their colleagues in the Torrance Research Center, in particular L. Hackett for electron-beam fabrication, J. Schellenberg for critical discussions and RF measurements, and T. Midford for continuing support.

References

[1] G. D. Alley, "Interdigital capacitors and their application to lumped element microwave circuit," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-18, pp. 1028–1033, Dec. 1970.

[2] J. L. Hobdell, "Optimization of interdigital capacitors," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-27, pp. 788–791, Sept. 1979.

[3] H. A. Wheeler, "Transmission-line properties of a strip on a dielectric sheet on a plane," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-25, pp. 631–641, Aug. 1977.

[4] G. I. Zysman and A. K. Johnson, "Coupled transmission lines networks in an inhomogeneous dielectric medium," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-17, pp. 753–759, Oct. 1969.

[5] J. I. Smith, "The even- and odd-mode capacitance parameters for coupled lines in suspended substrate," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-19, pp. 424–431, May 1971.

[6] R. H. Jansen, "High-speed computation of single and coupled microstrip parameters including dispersion, high order modes, loss and finite thickness," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 75–82, Feb. 1978.

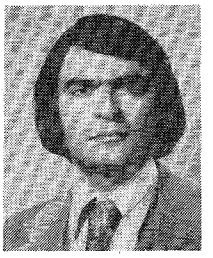
[7] H. A. Wheeler, "Formulas for skin effect," *Proc. IRE*, vol. 30, no. 9, pp. 412–424, Sept. 1942.

[8] M. Caulton, J. J. Hughes, and H. Sobol, "Measurement of the properties of microstrip transmission lines for microwave integrated circuit," *RCA Rev.*, vol. 27, no. 3, pp. 377–391, Sept. 1966.

[9] R. Horton, B. Easter, and A. Gopinath, "Variation of microstrip loss with thickness of strips," *Electron. Lett.*, vol. 7, no. 17, Aug. 1971.

[10] V. Rizzoli, "Losses in microstrip arrays," *Alta Freq.*, vol. XLVI, no. 2, pp. 86–94, Feb. 1975.

[11] G. L. Matthaei, L. Young, and E. M. T. Jones, *Microwave Filters, Impedance Matching Networks and Coupling Structure*. New York: McGraw-Hill, 1964.



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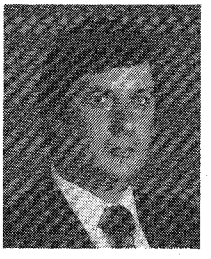

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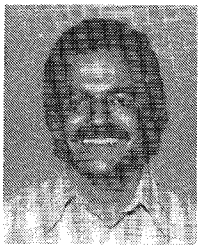

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